

S. B. Roll. No.....

VLSI SYSTEM DESIGN
6th Exam/ECE/3613/Nov'24
(For 2018 Batch Onwards)

Duration: 3Hrs.

M.Marks:75

SECTION-A

Q1. Do as directed.

15x1=15

- a. What are enumeration data types?
- b. What is clock?
- c. What is transport delay?
- d. List out the levels of abstractions in VHDL.
- e. Which is the Signal assignment operator?
- f. How many styles of loop statement does the VHDL have?
- g. FPGA stands for _____
- h. CPLD stands for _____
- i. VHDL stands for _____
- j. PAL stands for _____
- k. What kind of statement is the IF statement?
- l. Write the name of any two logical operators.
- m. Which is the high level representation of VLSI design?
- n. What is IEEE stands for?
- o. Which is the default mode for a Port variable?

SECTION-B

Q2. Attempt any six questions.

6x5=30

- i. Write the VHDL code for 4:1 multiplexer.
- ii. What do you understand by an entity?
- iii. Write down the advantage of HDL.
- iv. State the differences between Concurrent and Sequential statements.
- v. Compare CPLD and FPGA.
- vi. Write the VHDL code for the D Flip-flop.
- vii. Explain different data objects used in VHDL.
- viii. What are the basic design units in VHDL?
- ix. What is operator overloading? Explain its use in VHDL.

SECTION-C

Q3. Attempt any three questions.

3x10=30

- a. Compare behavioral, dataflow and structural modelling techniques.
- b. Write the VHDL code for the Full Adder.
- c. Explain the following i) CASE Statement — ii) IF Statement
- d. Explain ASIC Design flow with the help of block diagram.
- e. Explain the basic architecture of PLA. State its advantages, disadvantages and applications.